Nonlinear Effects In Oscillators and Synthesizers (Invited)

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***Abstract* --- This paper shows existing problems in VCO's and synthesizers due to the nonlinearities in the active device. I will propose design guidelines to minimize such effects in oscillators by using nonlinear design tools. In synthesizers, the reference frequency and its harmonics will mix with the output frequency in the phase detector and will cause spurious signals. A new method is proposed to introduce a synchronized jitter in the reference, which will remove these spurious frequencies far enough outside the loop bandwidth to be suppressed by at least 90dB.**

I. INTRODUCTION

Contrary to common discussions, oscillators, after reaching steady state, are not nonlinear in the common sense. While the collector current may show a distortion due to harmonic contents, the voltage across the resonator or even at the transistor is highly sinusoidal. The voltage dependent capacitances are nonlinear and the transconductance is a strong function of the collector/drain current. The active device is noisy, meaning that the various sources inside the transistor cause noise to appear and to be superimposed on the carrier of the oscillator. Both the conversion noise and the modulation noise are based on nonlinearities and were discussed in great detail by Rizzoli and Rohde.

The common source of noise in a bipolar transistor is the base spreading resistor and the base emitter diode (diode noise). In field effect transistors, the gate noise is a major source. For both devices, the flicker frequency component determines the low frequency noise. Here the problem lies in two areas:

1. the low DC-current flicker noise must not be confused with the large signal flicker noise as found in oscillators and mixers, and
2. the fact that the flicker noise contributions are bias dependent, mostly current dependent.

In the case of the VCO, the tuning diodes have to be operated in a saturation-free mode where their nonlinearity-based noise contribution will be kept at a minimum.

II. THE VCO

The VCO, in our example is a common Colpitts oscillator, as shown in Fig. 1. By adding an external inductance (8nH) between the capacitive divider from base to emitter, we have designed an oscillator. The second transistor labeled Q2 is used for DC stabilization and phase noise improvement. This approach was introduced already. The resulting negative resistance is calculated from

$$R_n = -\frac{\mathrm{Re}(Y_{21})}{\omega^2 \times C_1 \times C_2} \qquad (1)$$

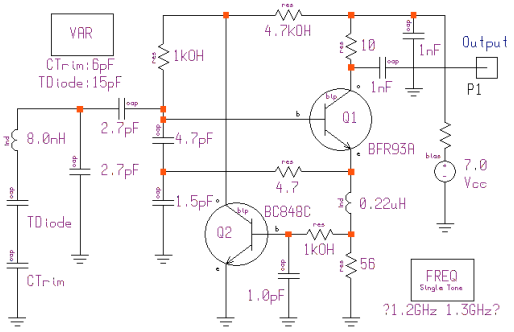

Figure 1. BJT-based oscillator with noise feedback. The noise sampling is done in the transistor emitter.

By analyzing both real and imaginary components at the base and assuming all things are linear, we obtain Fig. 2. In moving up in frequency, we find that a VCO, as shown in Fig. 3, is the design of choice and by applying the same test current method, we may obtain a curve as shown in Fig. 4.

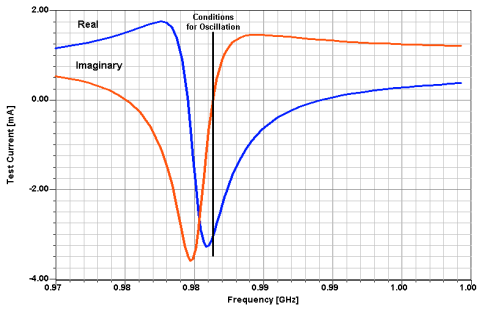

Figure 2. Real and imaginary values for Z_{11}. Real (Z_{11}) must be slightly more negative than the loss resistance in the circuit for oscillation to start. The resulting dc shift in the transistor will then provide the amplitude stabilization as g_m will be reduced. The steepness of the curve showing the test currents indicates a high operating Q that results in low phase noise. The steeper the slope at the changeover from inductive to capacitive reactance, the higher the resonator Q.

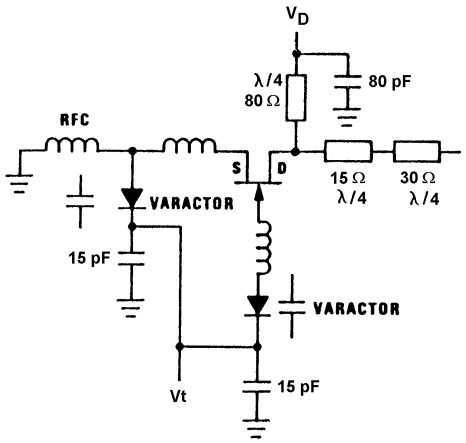

Figure 3. A microwave VCO, in which the output power is obtained from the collector.

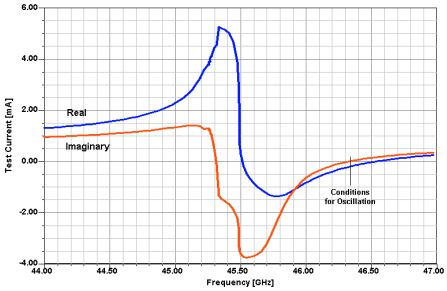

Figure 4. Test currents for finding the oscillating conditions of the 47GHz oscillator. The actual linear prediction is 46.3GHz; the large-signal condition then shifts the result towards 47GHz. The strange curves are due to the highly nonlinear operation, including the two transistors acting as tuning diodes.

The combination of the transistor and the tuning diode now results in a highly nonlinear test current behavior. Fig. 5 shows the overdrive at the DC IV curve. The left curve is a result of excessive drive and even the curve on the right side shows that the current displays negative values. Using an external AGC circuit, similar to Q2 in the previous circuit, Fig. 1, the output load line defaults to an ellipse. It needs to be noted that in this case neither the current nor the voltage show negative values. Needless to say, this can only be demonstrated by using a microwave simulator which has the appropriate nonlinear models, both bipolar and FET, and that the appropriate model parameters have been made available from the parameter extraction.

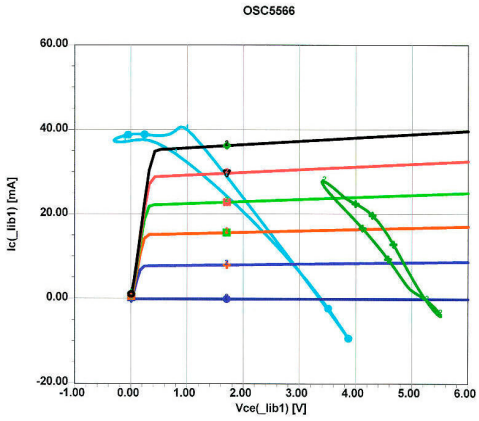

Figure 5. Load lines for overdrive (left) and medium drive (right). This circuit still exhibits negative currents.

Fig. 6 shows the output load line for this case. While this AGC action reduces the output power by only 2dB, the harmonic suppression went from 4dB to about 20dB. This means that the overdrive condition was cancelled. Fig. 7 shows this relationship between the two cases. On the other hand, the phase noise has been improved significantly, operating at a lower dissipation point. Fig. 8 shows a noise improve of almost 30dB based on this operating point. A further decrease in phase noise can be achieved if the characteristic impedance of the tuned circuit is less than 15Ω.

$$Z = \sqrt{L/C} \tag{2}$$

An even better phase noise improvement is achieved by replacing the inductor with a transmission line.

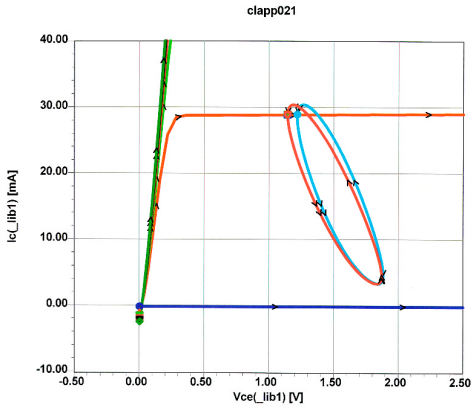

Figure 6. Perfect load line because of AGC control.

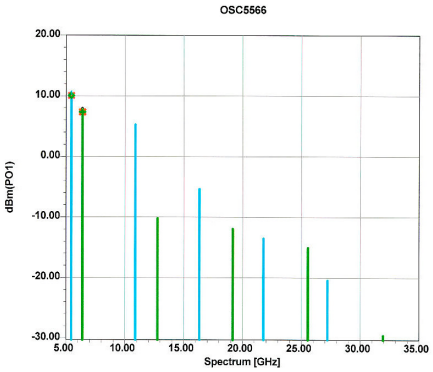

Figure 7. Reduction in harmonic controls when choosing a better bias current.

An additional method of reducing the second harmonic is the use of resonant capacitors in the Colpitts feedback, which provide a shunt of the harmonic components from base to ground. An international patent application for this has been filed in Europe, Asia, and the United States obtaining a wideband application. A somewhat frequency restricted form of this has been dealt with in the U.S. patent #5,144,264. Another interesting patent which was recently issued for a low noise oscillator is the U.S. patent #6,075,421, June 13, 2000. It uses a clever method of feedback, however, the purpose of having two transistors in parallel is not demonstrated in a useful fashion.

An additional design guidance is to use a bipolar transistor. Using I_C max is about 4-5 times the actual operating current and F_T should not be selected to be much higher than 6 times the operating frequency. The reason for the first recommendation lies in the bias dependent flicker noise, and the reason for the second recommendation lies in the fact that transistor manufacturers use stabilizing methods to make even 75GHz bipolar transistors stable at lower frequencies. This is done at the expense of low frequency noise figures, which would affect the oscillation. The flicker corner frequency increases with F_T. As to the determination of the oscillator frequency, a standard linear tool would not have shown the distortion in the test currents and even their oscillator frequency projection was incorrect. The nonlinear harmonic balance simulator was the only tool capable of delivering the frequency of oscillation within a few percent of the measured value. To be specific, the linear approach predicted 46.3GHz, while the actual measured frequency was 47GHz, which the nonlinear simulator correctly predicted.

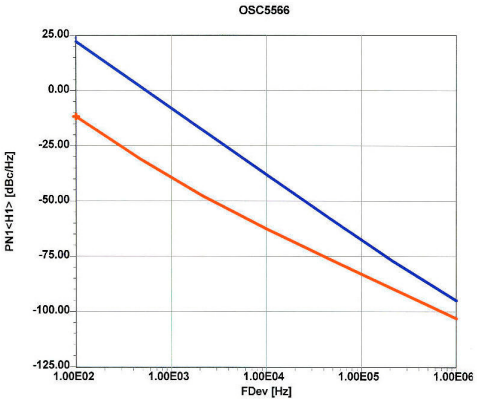

Figure 8. Noise improvement based on AGC action.

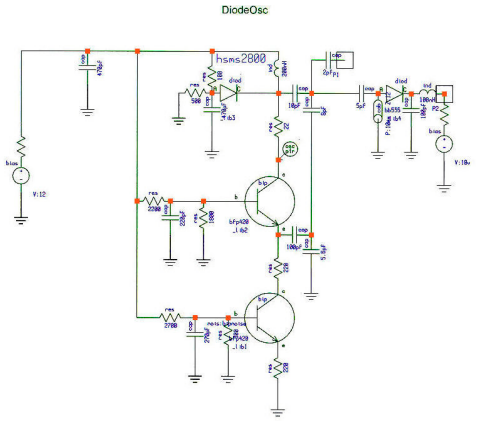

Figure 9. Ceramic resonator-based oscillator with hot carrier diode supplementing RF current which yields to better phase noise.

III. Nonlinear Effects And Spurious In Synthesizers

Frequency Synthesizers cannot reject spurious signals that appear inside the loop bandwidth. By introducing a jitter as the reference frequency, the unwanted spurious signal can be shifted far away from the loop filter so that it gets rejected by the loop filter of the synthesizer. This can be explained by the following example, where

reference frequency = 80MHz
output frequency = 670MHz
reference division number = 8 (before jitter)

In this case the comparison frequency will be 10mHz and the fractional division number will be 67, which is an integer. Shift the frequency by 1KHz to 670.001MHz and the division will be 67.0001; which gives us a spurious signal that is 1KHz away from the carrier and –45dBc.

A novel way to circumvent this problem is to add a jitter as the reference frequency, thereby, making the comparison frequency have an integer relationship with the output frequency. This scheme can be implemented by dividing the reference frequency by 8.5, where N, A, and B correspond to 8, 1 and 2, respectively, in (3).

$$N + (A/B) = \{(B-A)\,N+A\,(N+1)\}/B \qquad (3)$$

The new comparison frequency will be

$$\frac{80}{8.5} \cong 9.41176MHz$$

and the corresponding fractional division number will be approximately 71.1875, thus, providing the required frequency of 670.001MHz. It is evident that the output frequency is not close to integral multiple of the comparison frequency.

The new spurious signal will be approximately $0.5 \times 9.41126 = 4.705$MHz away from the center frequency and be rejected by the loop filter. This spurious signal is typically 80dBc down from the carrier.

IV. Conclusion

Due to the ridiculous space restrictions of only four pages for such a complex topic, I have posted this paper, in full length, on the website www.synergymwave.com, under the heading of Publications, at the time of the MTT.